2.5V Drive Nch+Nch MOS FET UM5K1N

Structure

Silicon N-channel MOS FET

Features

- 1) Two 2SK3018 transistors in a single UMT package.
- 2) Mounting cost and area can be cut in half.
- 3) Low on-resistance.
- 4) Low voltage drive (2.5V) makes this device ideal for portable equipment.
- 5) Drive circuits can be simple.

Abbreviated symbol : K1

●External dimensions (Unit : mm)

UMT5

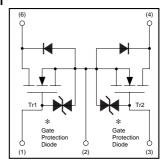
Applications

Interfacing, switching (30V, 100mA)

Packaging specifications

Туре	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
UM5K1N		0

●Equivalent circui



- (1) Tr1 Gate (2) Source (3) Tr2 Gate (4) Tr2 Drain (6) Tr1 Drain
- * A protection diode has been built in between the gate and the source to protect against static electricity when the product is in use. Use the protection circuit when rated voltages are exceeded.

● Absolute maximum ratings (Ta=25°C)

<It is the same ratings for Tr1 and Tr2.>

Parameter		Symbol	Limits	Unit	
Drain-source voltage		Voss	30	V	
Gate-source voltage		Vgss	±20	V	
Drain current	Continuous	lo	±100	mA	
	Pulsed	IDP*1	±400	mA	
Total power dissipation		Pp*2	150	mW / TOTAL	
		FD	120	mW / ELEMENT	
Channel temperature		Tch	150	°C	
Storage temperature		Tstg	-55 to +150	°C	

^{*1} Pw≤10μs, Duty cycle≤50%

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	Rth(ch-a)*	833	°C / W / TOTAL
Charline to ambient		1042	°C / W / ELEMENT

^{*} With each pin mounted on the recommended lands.

^{*2} With each pin mounted on the recommended lands.

●Electrical characteristics (Ta=25°C)

<It is the same characteristics for Tr1 and Tr2.>

Parameter	Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Gate-source leakage	Igss	-	-	±1	μΑ	Vgs=±20V, Vds=0V
Drain-source breakdown voltage	V _{(BR)DSS}	30	_	_	V	ID=10μA, VGS=0V
Zero gate voltage drain current	IDSS	I	-	1	μΑ	V _{DS} =30V, V _{GS} =0V
Gate threshold voltage	VGS(th)	0.8	-	1.5	V	V _{DS} =3V, I _D =100μA
Static drain-source on-stage	RDS(on)	_	5	8	Ω	In=10mA, Vgs=4V
resistance	RDS(on)	-	7	13	Ω	ID=1mA, VGS=2.5V
Forward transfer admittance	Yfs	20	-	_	mS	In=10mA, Vns=3V
Input capacitance	Ciss	_	13	_	pF	V _{DS} =5V
Output capacitance	Coss	_	9	_	pF	Vgs=0V
Reverse transfer capacitance	Crss	_	4	_	pF	f=1MHz
Turn-on delay time	td(on)	_	15	_	ns	In=10mA, Vnn≒5V
Rise time	tr	_	35	_	ns	Vgs=5V
Turn-off delay time	td(off)	-	80	_	ns	RL=500Ω
Fall time	tr	_	80	_	ns	R _G =10Ω

•Electrical characteristic curves

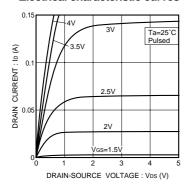


Fig.1 Typical output characteristics

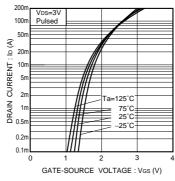


Fig.2 Typical transfer characteristics

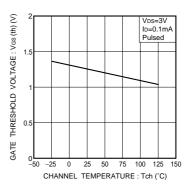


Fig.3 Gate threshold voltage vs. channel temperature

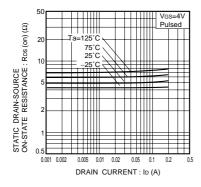


Fig.4 Static drain-source on-state resistance vs. drain current (I)

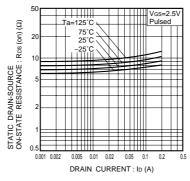


Fig.5 Static drain-source on-state resistance vs. drain current (II)

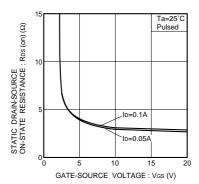


Fig.6 Static drain-source on-state resistance vs. gate-source voltage

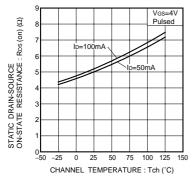


Fig.7 Static drain-source on-state resistance vs. channel temperature

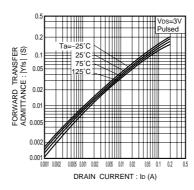


Fig.8 Forward transfer admittance vs. drain current

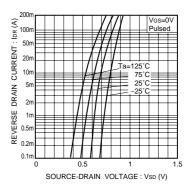


Fig.9 Reverse drain current vs. source-drain voltage (I)

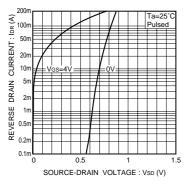


Fig.10 Reverse drain current vs. source-drain voltage (II)

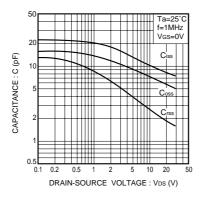


Fig.11 Typical capacitance vs. drain-source voltage

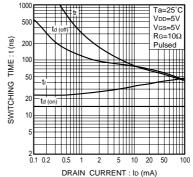


Fig.12 Switching characteristics (See Figures 13 and 14 for the measurment circuit and resultant waveforms)

Switching characteristics measurement circuit

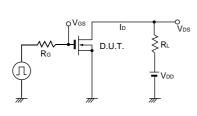


Fig.13 Switching time measurement circuit

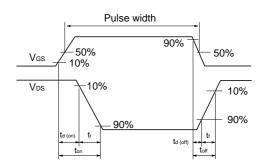


Fig.14 Switching time waveforms

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